Sub A1

<u>What is claimed is</u>:

1. A method for recovering phase information comprising:

over-sampling data transmitted at a first frequency using a clock at a second frequency to obtain groups of n samples;

storing a plurality of m of said groups of n samples;

outputting said plurality of m of said groups of n samples simultaneously at a clock frequency which is said second frequency divided by m.

2. A method according to claim 1 and further including:

using said plurality of m of said groups of n samples to detect transitions in said data; and

maintaining an historical record of said transitions.

3. A method according to claim 2 and further including:

using said historical record to determine a phase of said second frequency that is nearly centered in the middle of a bit time of said data at said first frequency.

4. A method according to claim 3 wherein said step of determining a phase comprises:

a. Oring each history bit with the following bit to obtain a highest byte;

b. Oring each bit in said highest byte with a bit on either side to obtain a second highest byte;

c. Oring each bit in said second highest byte with a bit on either side to obtain a third highest byte; and

d. determining the highest level byte which has two or fewer zeros and outputting:

   i. the phase of the sole remaining zero if there is only one zero;

   ii. the phase of the latest zero if an adjacent pair remains;

   iii. an error indication if two non-adjacent zeros remain.

5. A method according to claim 4 and further including limiting the maximum phase change to plus or minus one sample phase.

6. A method according to claim 3 and further including:

using said historical record to select bits of said data at said first frequency and output said bits in groups of generally m valid bits at a time at said second frequency divided by m.

7. A method according to claim 6 wherein, due to the difference in said first and second frequency a draft occurs causing said phase to select m+1 or m-1 bits of data and further including:

outputting either m, m+1 or m-1 valid bits; and

using said historical record to provide an indication of how many bits are being output.

8. A method according to claim 7 wherein said step of providing an indication of how many valid bits are being output comprises:

a. determining whether the current phase selection is different from the previous phase selection and if not, indicating that bits m:1 are valid;

b. if the current phase selection is different from the previous phase selection, determining if the current phase selection wraps around from the previous phase selection and if not, indicating that bits m:1 are valid;

c. if the current phase selection wraps around from the previous phase selection determining if it wraps around from the latest to earliest sample phase, and, if so, indicating that bits (m-1):1 are valid; and

d. if the current phase selection wraps around from the previous phase selection determining if it wraps around from the earliest to latest sample phase, and, if so, indicating that bits m:0 are valid.

9. A method for recovering phase information comprising:

over-sampling data transmitted at a first frequency using a clock at a second frequency, n times per bit time to obtain n samples;

using said n samples to detect the transitions between two logic levels in said transmitted data an provide n edge results which are at one logic level to indicate a transition and the other logic level to indicate no transition;

storing, in sequence, at said second clock frequency, m sets of said n samples; and

outputting said m times n samples at a clock frequency which is said second frequency divided by m.

10. A method according to claim 9 and further including maintaining a running history of said edge results comprising:

combining in n separate m input OR gates the m times n samples, each gate having as inputs the m of said samples in the same relative position in each of said m sets;

using the outputs of said n OR gates to set p sets of byte registers, each having n registers; and

resetting said p byte registers in a wrap around sequence.

11. A method according to claim 10 and further including:

using outputs of said byte registers to determine a phase of said second frequency that is nearly centered in the middle of a bit time of said data at said first frequency.

12. A method according to claim 11 wherein said step of determining a phase comprises:

a. Oring each history bit with the following bit to obtain a highest byte;

b. Oring each bit in said highest byte with a bit on either side to obtain a second highest byte;

c. Oring each bit in said second highest byte with a bit on either side to obtain a third highest byte; and

d. determining the highest level byte which has two or fewer zeros and outputting:

i. the phase of the sole remaining zero if there is only one zero;

ii. the phase of the latest zero if an adjacent pair remains;

iii. an error indication if two non-adjacent zeros remain.

13. A method according to claim 12 and further including limiting the maximum phase change to plus or minus one sample phase.

14. A method according to claim 13 and further including:

using said phase to select bits of said data at said first frequency and output said bits in groups of generally m at a time at said second frequency divided by m.

15. A method according to claim 14 wherein, due to the difference in said first and second frequency a drift occurs causing said phase to select m+1 or m-1 bits of data and further including:

outputting either m, m+1 or m-1 bits; and

using said phase information to provide an indication of how many bits are being output.

16. A method according to claim 15 wherein said step of providing an indication of how many bits are being output comprises:

a. determining whether the current phase selection is different from the previous phase selection and if not, indicating that bits m:1 are valid;

b. if the current phase selection is different from the previous phase selection, determining if the current phase selection wraps around from the previous phase selection and if not, indicating that bits m:1 are valid;

c. if the current phase selection wraps around from the previous phase selection determining if it wraps around from the latest to earliest sample phase, and, if so, indicating that bits m-1:1 are valid; and

d. if the current phase selection wraps around from the previous phase selection determining if it wraps around from the earliest to latest sample phase, and, if so, indicating that bits m:0 are valid.

17. Apparatus for recovering phase information comprising:

an over-sampler having an input for data transmitted at a first frequency and n sampling clock inputs each at a second frequency but different phase each clock shifted in phase from an adjacent clock by 360/n degrees and providing n sample outputs; and

a sample word register having inputs coupled to said n sample outputs, storing m sets of said n sample outputs at said second frequency and outputting said m sets of n sample outputs at a frequency equal to said frequency divided by m.

18. Apparatus according to claim 18 and further including an edge detector using said m sets of n sample outputs to detect the transitions between two logic levels in said transmitted data and provide m sets of n edge results which are at one logic level to indicate a transition and another logic level to indicate no transition.

19. Apparatus according to claim 18 wherein said edge detectors comprise a plurality of XOR gates.

20. Apparatus according to claim 19 and further including:

n separate m input OR gates, each gate having as inputs the m of said n edge results in the same relative position in each of said m sets of n edge results; and

p sets of n-bit byte registers, the outputs of each of said n OR gates being a set input to one of the n bits in each of said p byte registers.

21. Apparatus according to claim 20 and further including a packet state machine providing reset inputs to said byte registers.

22. Apparatus according to claim 21 and further including:

phase selection logic having the outputs of said byte registers as inputs and outputting a signal indicating a phase of said second frequency that is nearly centered in the middle of a bit time of said data at said first frequency.

23. Apparatus according to claim 22 and further including:

a data selector register having a data input from said sample register and the output of said phase selection logic as a select input to select bits of said data at said first frequency and output said bits in groups of generally m valid bits at a time at said second frequency divided by m.

24. Apparatus according to claim 23 wherein due to the difference in said first and second frequency a drift occurs casing said data selector register to output m+1 or m-1 valid bits of data and further including:

a bit count state machine providing as an output an indication of how many valid bits are being output by said data selector register.